

1

SEMICONDUCTOR SWITCHING DEVICE INCLUDING CHARGE STORAGE STRUCTURE

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority to German Application No. 102014111981.9, filed on Aug. 21, 2014, and incorporated herein by reference in its entirety.

BACKGROUND

Power semiconductor switching devices are either normally-on devices conducting a load current in the absence of a potential difference between gate and source or normally-off devices which do not conduct a load current in the absence of a potential difference between gate and source. Inter alia for safety reasons normally-off switching devices are more popular. On the other hand in some applications, such as cascode circuits, normally-on switching semiconductor devices can reduce circuit complexity.

Further in the field of power semiconductor switching devices a desaturation cycle may partly reduce a charge carrier plasma before switching the semiconductor switching device from an on-state to a blocking state.

SUMMARY

It is an object to provide normally-on semiconductor switching devices as well as desaturable semiconductor switching devices with improved device characteristics.

According to an embodiment a semiconductor switching device includes a first load terminal electrically connected to source zones of transistor cells. The source zones form first pn junctions with body zones. A second load terminal is electrically connected to a drain construction that forms second pn junctions with the body zones. Control structures, which include a control electrode and charge storage structures, directly adjoin the body zones. The control electrode controls a load current through the body zones. The charge storage structures insulate the control electrode from the body zones and contain a control charge adapted to induce inversion channels in the body zones in the absence of a potential difference between the control electrode and the first load electrode.

According to another embodiment a semiconductor switching device includes transistor cells that include source zones forming first pn-junctions with body zones. The body zones form second pn-junctions with a drain construction. Auxiliary cells include charge carrier transfer zones that form third pn-junctions with desaturation portions of the drain construction. A first control structure includes a first portion of a control electrode and induces an inversion channel through the body zones in an on-state. A second control structure directly adjoins the desaturation portions of the drain construction. The second control structure includes a second portion of the control electrode and a charged layer sandwiched between the second portion of the control electrode and the desaturation portions. The charged layer contains a control charge adapted to induce an inversion layer in the desaturation portions in the on-state.

Those skilled in the art will recognize additional features and advantages upon reading the following detailed description and on viewing the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention and are incorporated

2

in and constitute a part of this specification. The drawings illustrate the embodiments of the present invention and together with the description serve to explain principles of the invention. Other embodiments of the invention and intended advantages will be readily appreciated as they become better understood by reference to the following detailed description.

FIG. 1A is a schematic cross-sectional view of a portion of a semiconductor switching device for illustrating effects of embodiments concerning normally-on semiconductor switching devices.

FIG. 1B are schematic IL/VGS characteristics for discussing effects of embodiments concerning normally-on semiconductor switching devices.

FIG. 2A is a schematic cross-sectional view of a portion of a semiconductor switching device according to an embodiment related to fixed charge carriers in a control dielectric of a normally-on semiconductor switching device.

FIG. 2B is a schematic cross-sectional view of a portion of a semiconductor switching device in accordance with an embodiment related to charges trapped in a dielectric charge trapping layer of a normally-on semiconductor switching device.

FIG. 2C is a schematic cross-sectional view of a portion of a semiconductor switching device in accordance with an embodiment related to a conductive charge storage layer of a normally-on semiconductor switching device.

FIG. 2D is a schematic cross-sectional view of a portion of a semiconductor switching device in accordance with an embodiment concerning normally-on semiconductor switching devices including a program electrode.

FIG. 3A is a schematic perspective view of a portion of a semiconductor switching device in accordance with an embodiment related to normally-on semiconductor switching devices with planar gate structures.

FIG. 3B is a schematic perspective view of a portion of a semiconductor switching device in accordance with an embodiment related to normally-on semiconductor switching devices with trench gate structures.

FIG. 3C is a schematic perspective view of a portion of a semiconductor switching device in accordance with an embodiment related to normally-on semiconductor switching devices based on FinFET (fin field effect transistor) cells.

FIG. 4A is a schematic circuit diagram of an electronic circuit including a normally-on semiconductor switching device according to an embodiment.

FIG. 4B is a schematic circuit diagram of an electronic circuit including a normally-on semiconductor switching device according to a further embodiment related to cascode circuits.

FIG. 5 is a schematic diagram plotting the drain current I_D as a function of the gate-to-source voltage V_{GS} and a control charge on a floating gate for discussing effects of embodiments concerning normally-on semiconductor switching devices.

FIG. 6 is a schematic diagram plotting a charge on a floating gate structure as a function of a charging time for discussing effects of embodiments concerning normally-on semiconductor switching devices as well as desaturable semiconductor switching devices.

FIG. 7A is a schematic cross-sectional view of a portion of a semiconductor switching device for illustrating effects of embodiments concerning desaturable semiconductor switching devices.

FIG. 7B is a schematic time chart for illustrating a mode of operation of the semiconductor switching device of FIG. 7A.